THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A Dynamic Random Access Memory (DRAM) for performing read, write, and refresh operations, said DRAM comprising:
   (a) a plurality of sub-arrays, each having a plurality of memory cells, each of which is coupled with a complementary bit line pair and a word line;
   (b) a word line enable device for asserting a selected one of said word lines;
   (c) a column select device for asserting a selected one of said bit line pairs;
   (d) a timing circuit for controlling said word line enable device, said column select device, and said read, write, and refresh operations in response to a word line timing pulse, wherein said read, write, and refresh operation are performed in the same amount of time.

2. A memory device for storing data in address locations specified input addresses, said memory device responsive only to read, write and refresh commands, each of said commands having a uniform latency independent of said input addresses.

3. A memory device as defined in claim 2 wherein said memory device comprises a dynamic random access memory (DRAM).

4. A memory device as defined in claim 2 wherein said memory device comprises an embedded dynamic random access memory (DRAM) macrocell.

5. A memory device as in claim 2 wherein independent of input address said read command includes a full row access operation comprising the steps of:
   (a) bit line pre-charge and equalization;
   (b) word line address decoding and word line assertion;
   (c) memory cell access to an associated bit line pair;
   (d) bit line sensing;
   (e) memory cell restoration; and
   (f) word line de-assertion.

6. A memory device as defined in claim 2 wherein said memory device is capable of receiving a new command on every leading edge of a system clock.

7. A memory device as in claim 2 wherein said memory device is capable of performing a read and write operation in a single system clock cycle in response to a simultaneous read/write command.

8. A memory device as in claim 7 wherein said simultaneous read/write operation comprises performing a write operation during a first portion of row cycle while bit line sense amplifiers are amplifying differential voltage on selected bit lines and before full differential voltage levels are established on said bit lines.

9. A memory device as in claim 5 wherein said steps of word line address decoding and bit line precharge and equalizing are performed substantially simultaneously during a first portion of a row cycle.

10. A method for performing a read command in a memory device in synchronization with a system clock comprising the steps of:
    (a) generating a main self-timed pulse derived from the system clock; and
    (b) generating a plurality of self-timed pulses activated in cascade based on said main self-timed pulse for controlling operation of address and data circuits.

11. A method for performing a read command as in claim 10 wherein said plurality of self-timed pulses comprises a first self-timed pulse for activating a selected sense amplifier power supply and a second self-timed pulse generated from said first self-timed pulse for activating a local memory column.